2152 37

iddqd2001

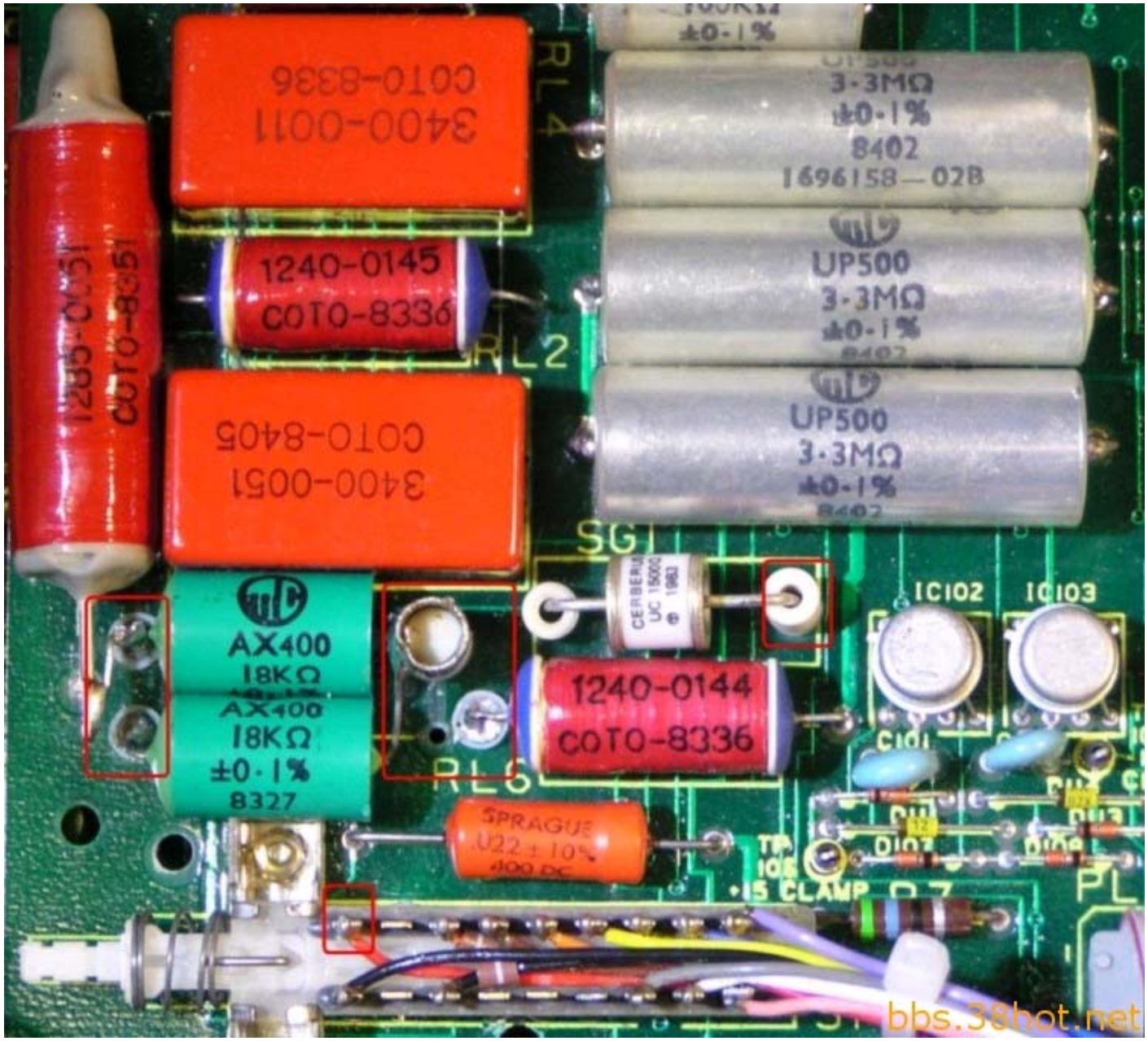
[ ]Solartron 7081 Repairing (continue) [ ]

0 : 2012-01-08

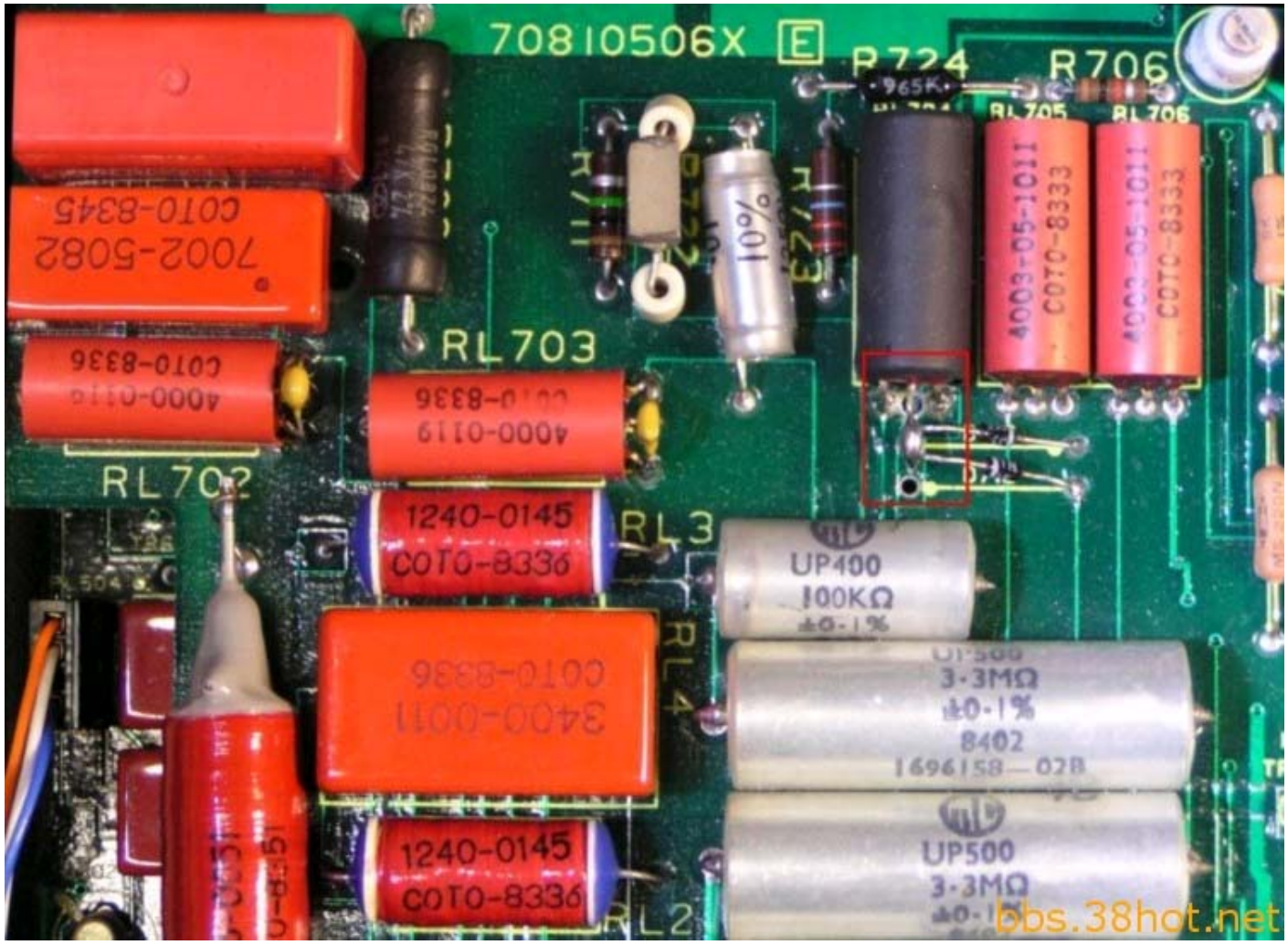
— yjm2000 (2012-01-08) —

Previous part: http://bbs.38hot.net/read.php?tid=12456

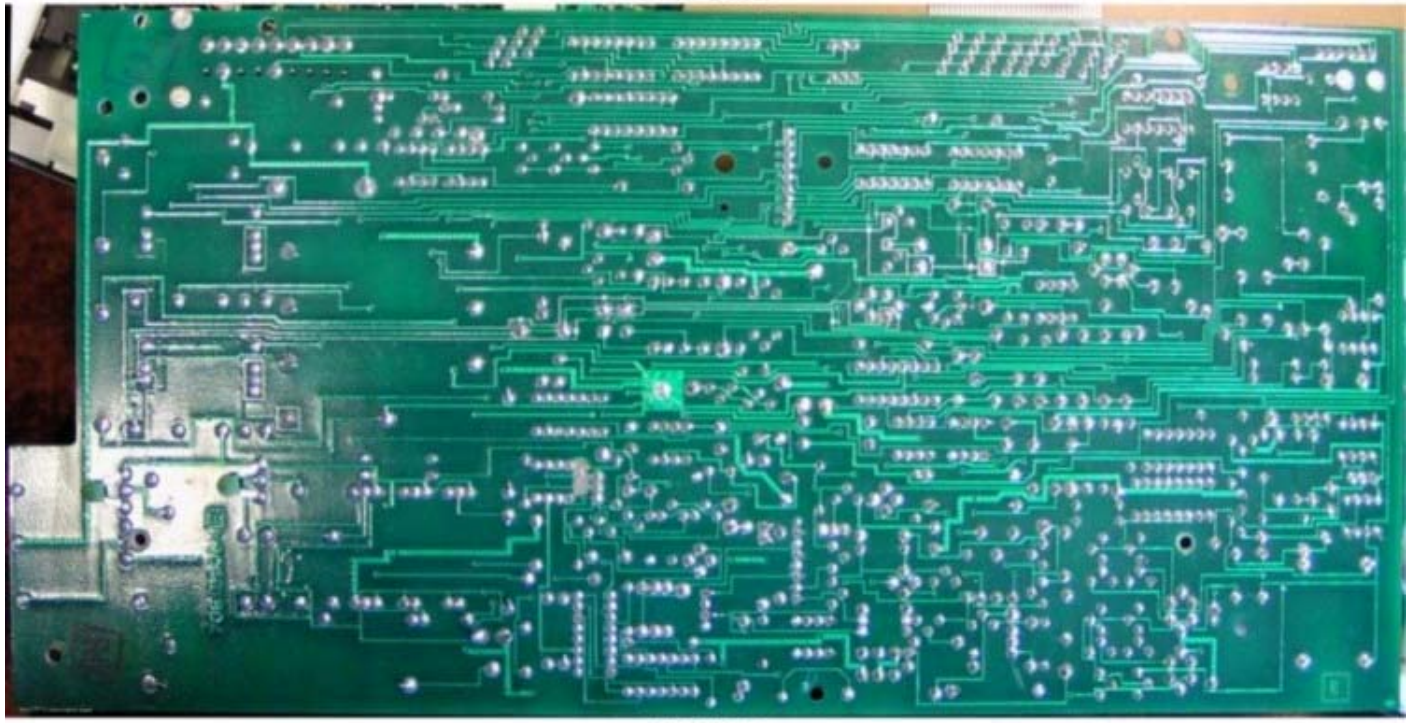
Three month ago I was purchase a Solartron 7081 DMM. It's one of the first model, dated Apr. 1984.
1) My tests showed a huge input bias current and suspiciously large noise. After 8 hours of heating at 25 Celsius degrees input current was 330 pA causing a zero shift in the short-circuited input – 12 uV. After checking each critical item in the input circuits (attenuator, DC ranging, input amplifier with MDM channel) and installing the PTFE bushings and insulators input bias has been reduced down to 1-2 pA!


3400-0011
C010-8336
3·3MΩ
±0·1%
8402
1696158—02B
1240-0145
C0T0-8336
UP500
3·3MΩ
±0·1%
UP500
3·3MΩ
±0·1%
3400-0051
C0T0-8405
AX400
18KΩ
AX400
18KΩ
±0·1%
8327
1240-0144
C0T0-8336
SPRAGUE
IC102
IC103
RL4
RL2
RL6
SG
bbs.38hot.net

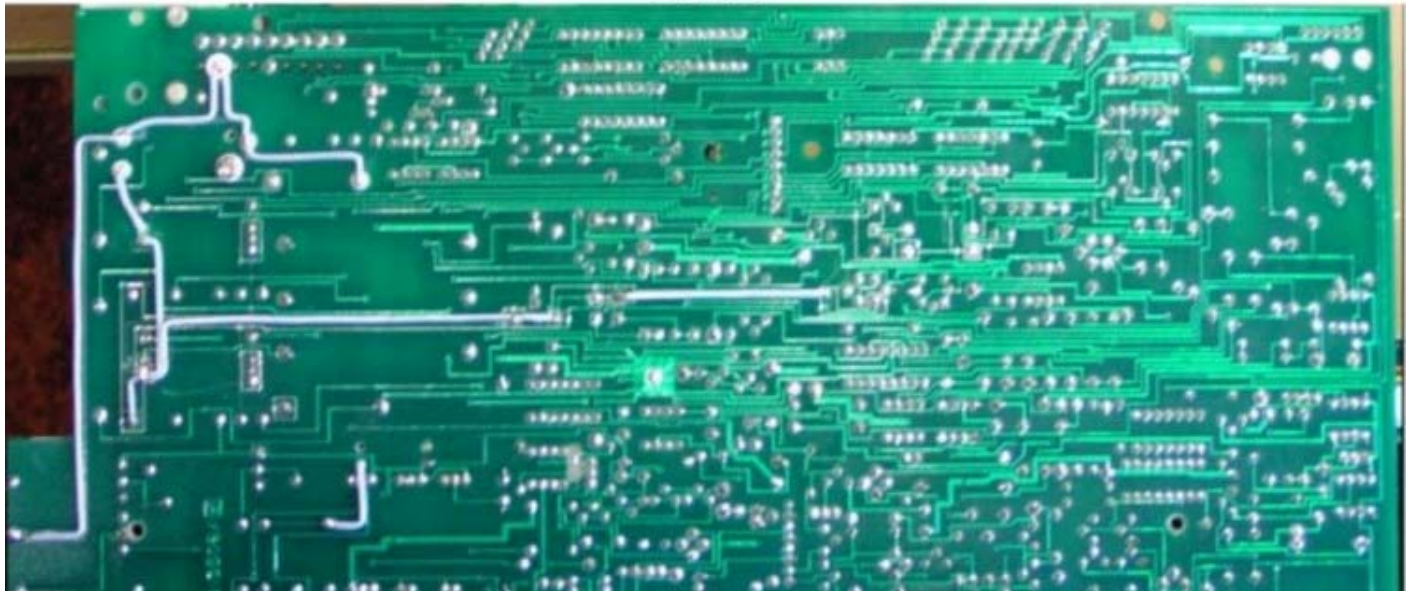
100
334
38


70810506X
E
R724
R706
RL705
RL706
RL703
RL702
RL3
RL4
RL2
1240-0145
C0T0-8336
UP400
100KΩ
±0·1%
3·3MΩ
±0·1%
8402
1696158—02B
UP500
3·3MΩ
bbs.38hot.net

BEFORE

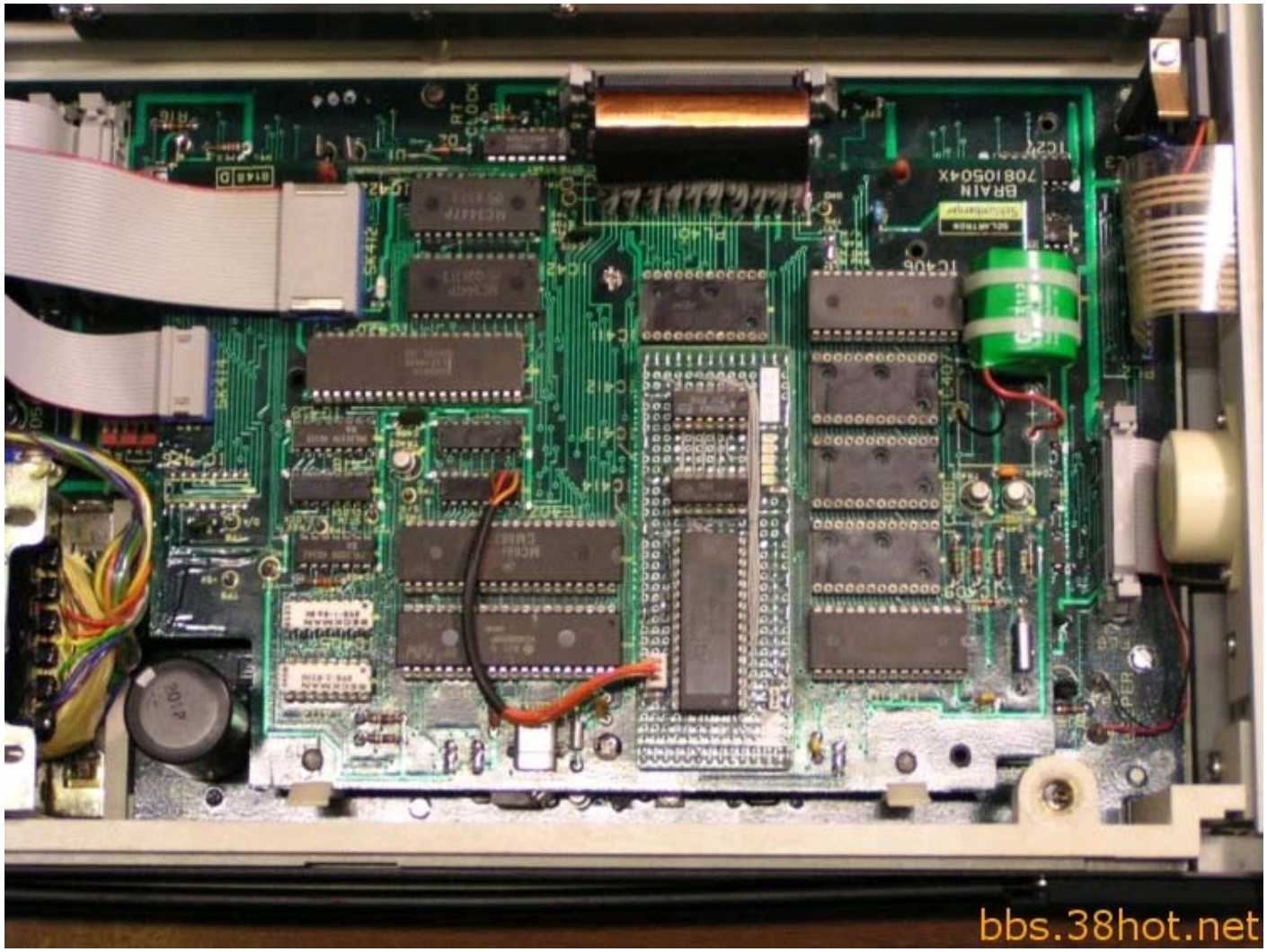


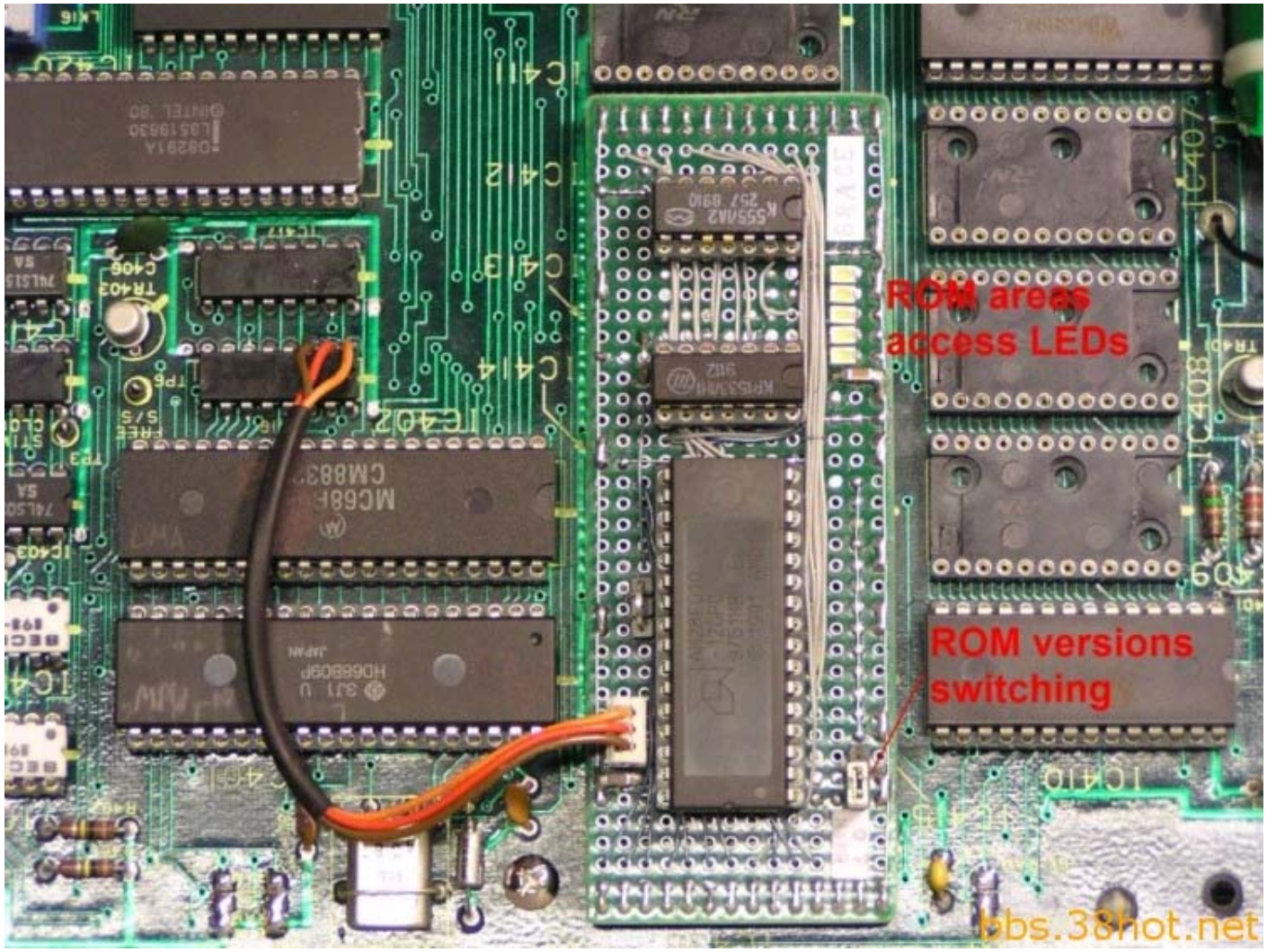
AFTER



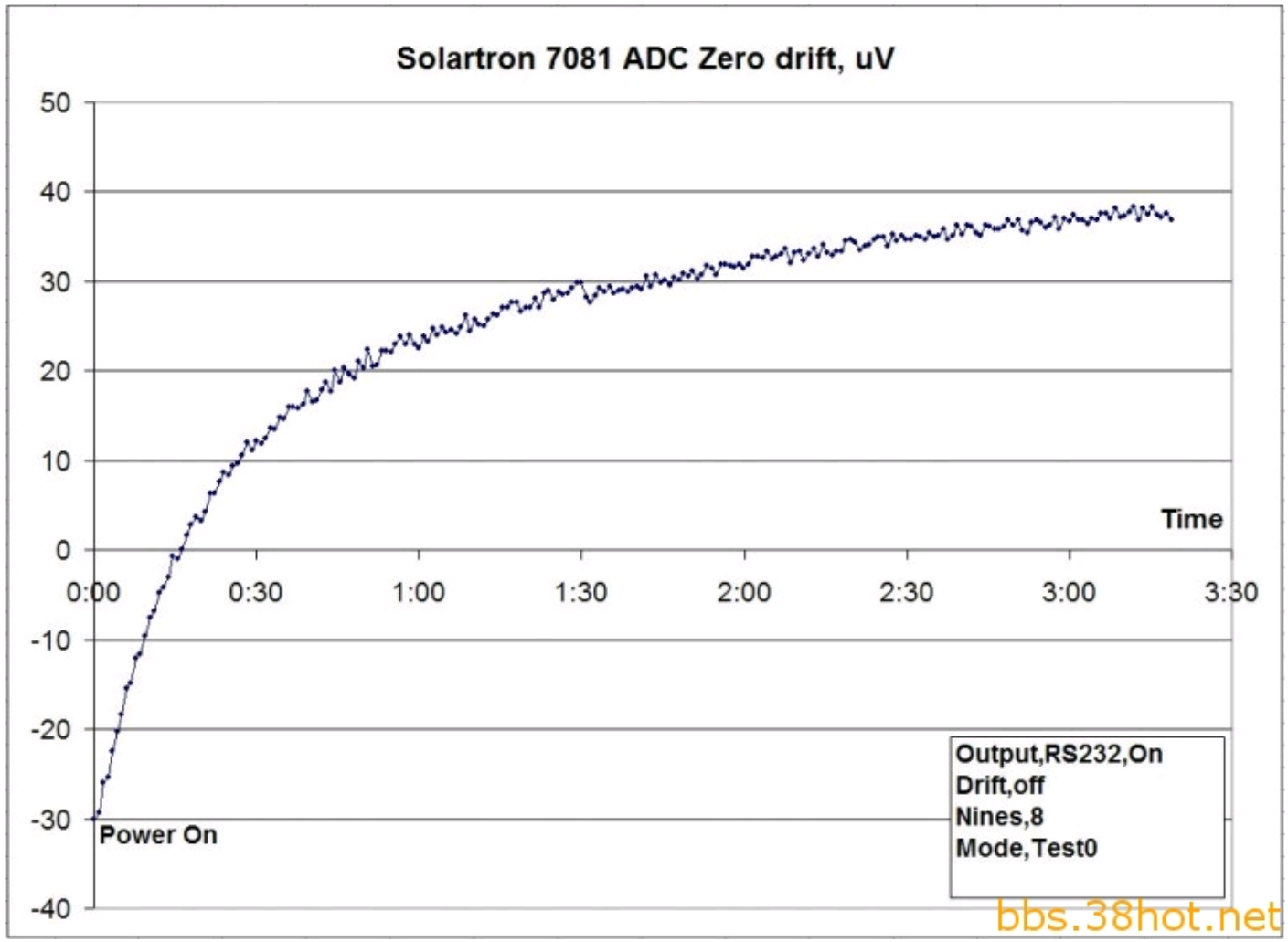
2) After six weeks my Solartron 7081 became very ill: no LED signs, no display, no life at all. I'm spent amount of time to research Earthy Logic and Processor boards, I/O and memory map, disassemble some of the early ROM procedures, emulate 7081 firmware via 6809 CPU emulator, change RAM/ROM chips decoding structure to replace the old and rare 2564 and 6117 chips and adopt PCB for new 28F010 and 6264 ones. I'm recompiling all of the 2564 ROM contents (1984 year) to the linear block and add to it recompiled ROMs content by Dave Partridge (1986 year) and flash its to the one 28F010 EEPROM. Now the DMM came to life again and I'm continue to research the ADC and analog subsystem. This is the replaced parts, including old and broken boards interconnection cable, two semi-defective RAM and ROM chips:

This is the new sub-PCB with two banked ROM 28F010 and address decoders:

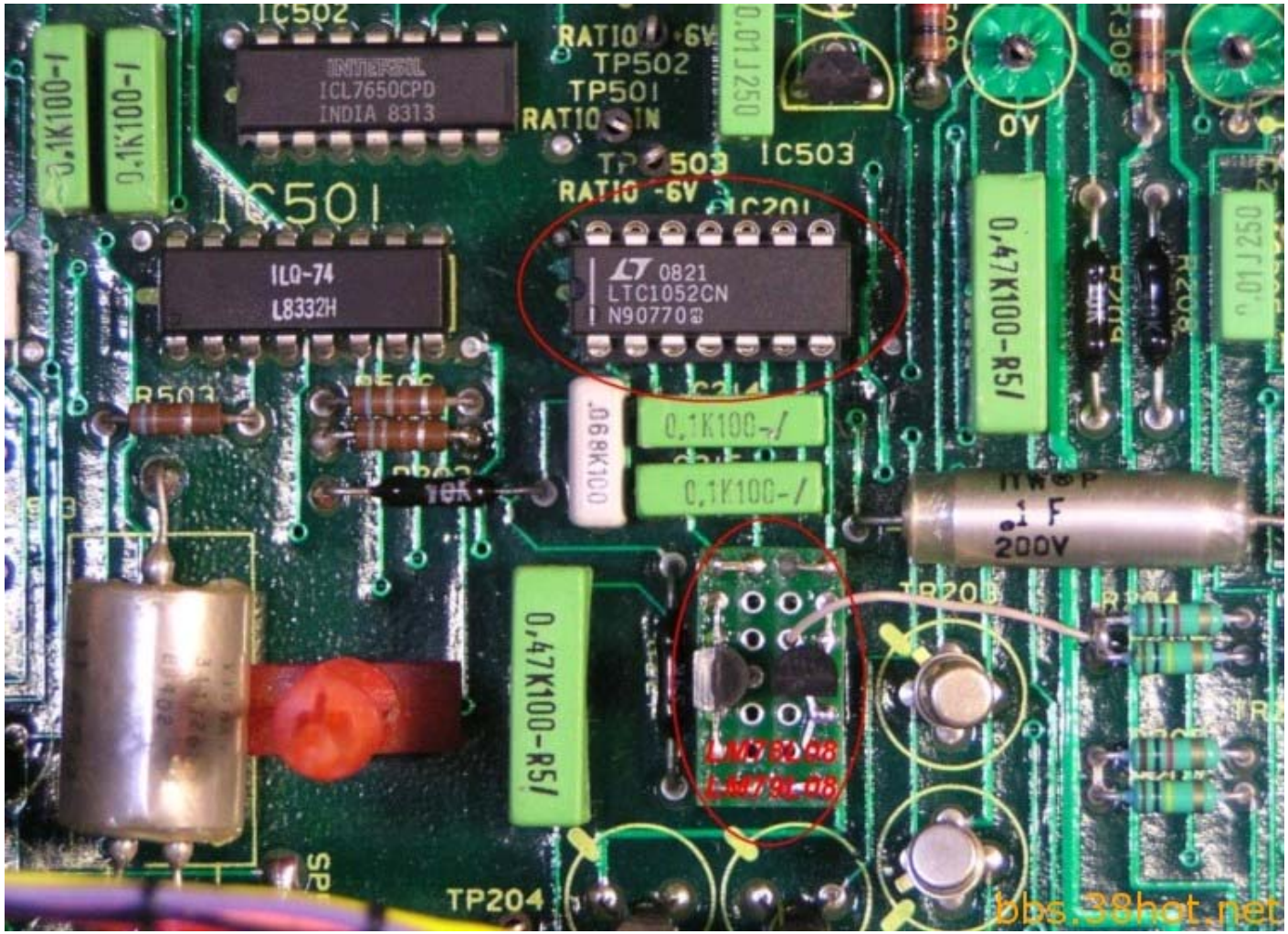

BRAIN
708105041X
bbs.38hot.net



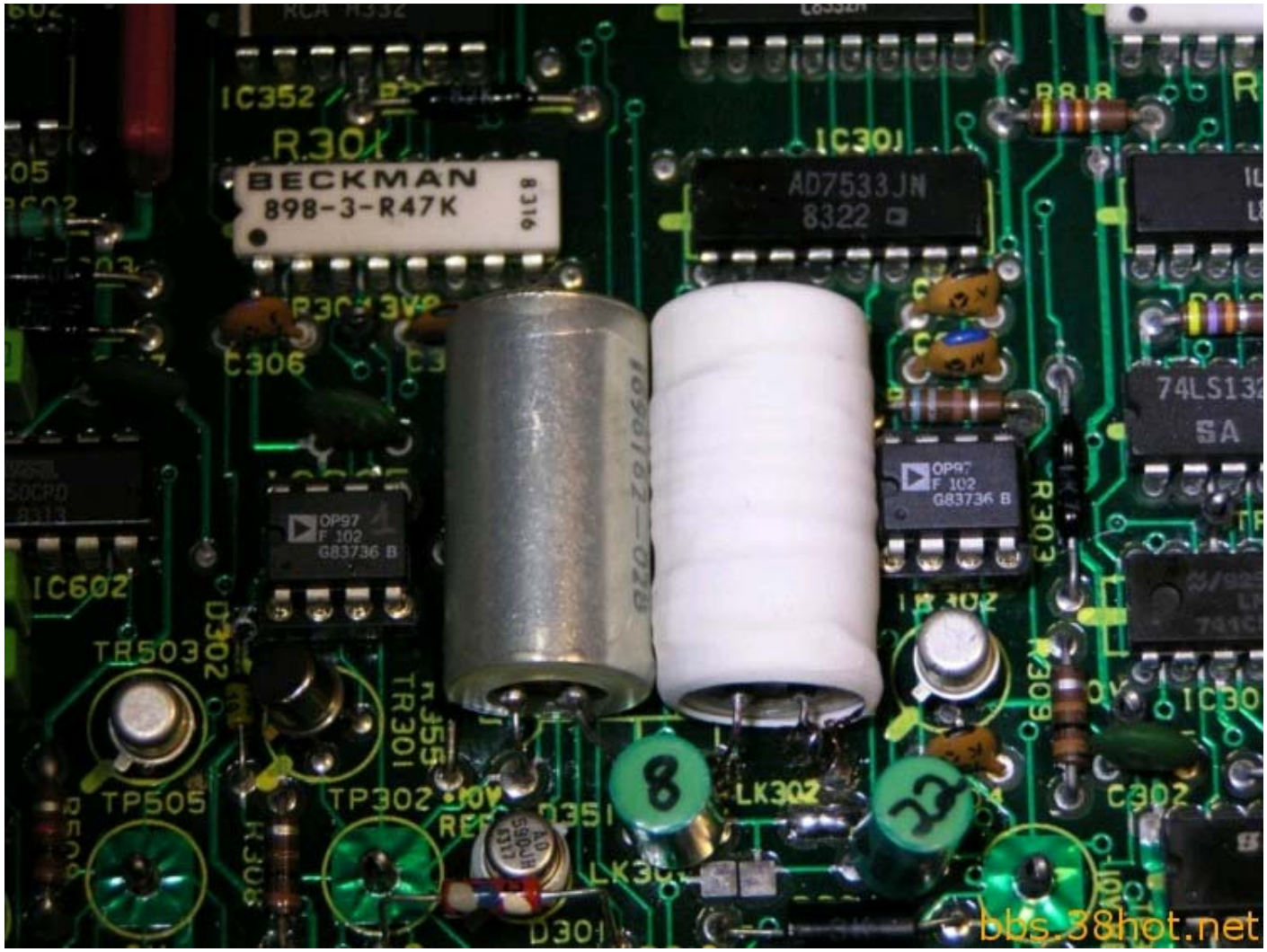
3) Next problem – extremely high ADC zero drift during 2-3 hours after the power up (up to 70 uV = 7ppm).

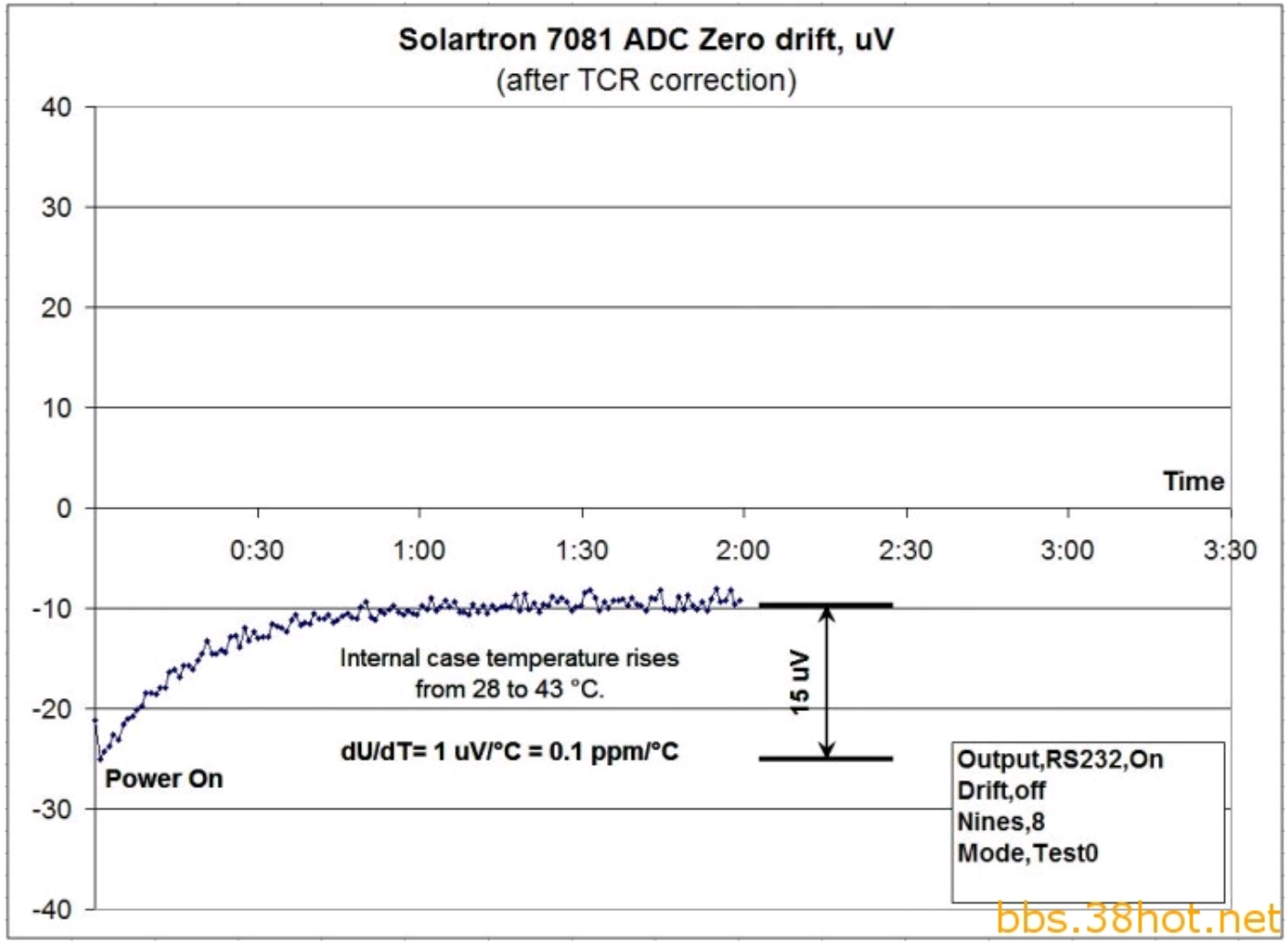


After the change of the integrators DC path op-amp ICL7650CPD to LTC1052CN, reference op-amps OP07EZ to selected OP97F, and after correction of the TCR of the reference divider with Cu wire the Solartron 7081 ADC zero drift was reduced to 15 uV (is equivalent to 0.1 ppm/C).

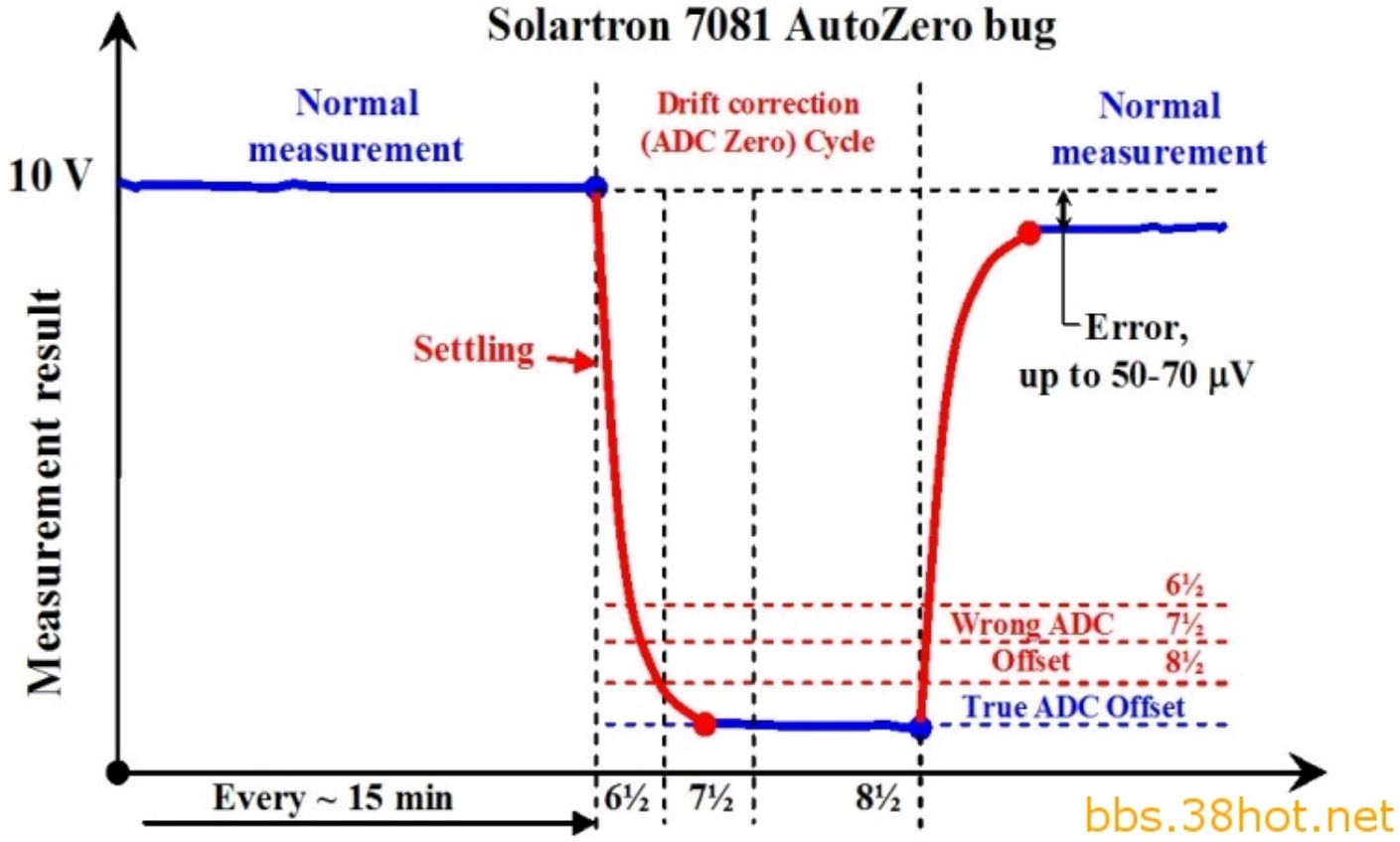

IC502
INTERSIL
ICL7650CPD
INDIA 8313
RATIO -6V
TP502
TP501
RATIO IN
TP503
IC503
RATIO -6V
IC501
IC201
ILQ-74
L8332H
0821
LTC1052CN
N90770
0V
0,47K100-R5/
0,1K100-/
0,1K100-/
.068K100
0,47K100-R5/
200V
TP204
bbs.38hot.net

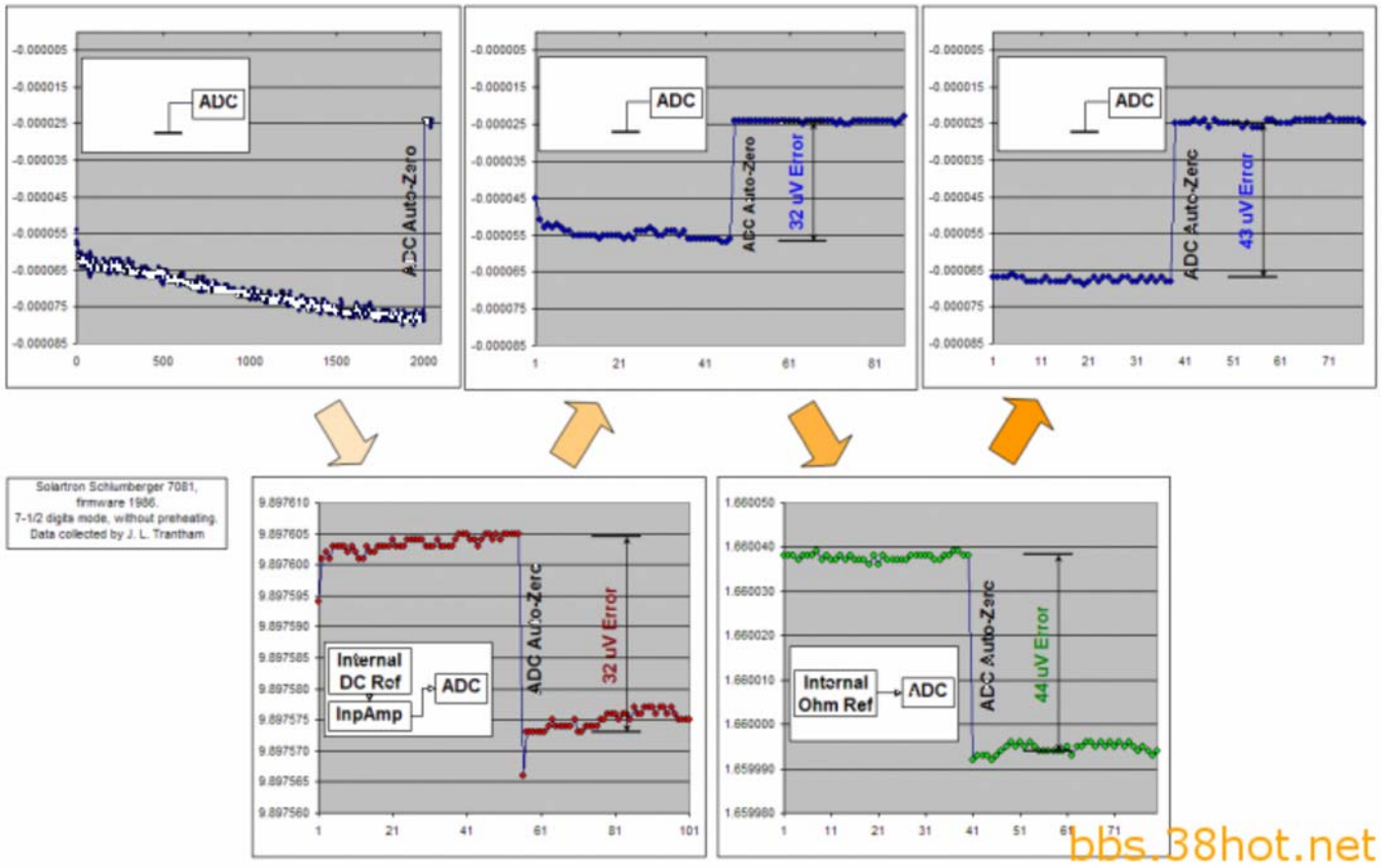

Если переключать на Test0 вручную,
В DMM_Mode_Table для Test0
В процедуре
Zero_On :
Не срабатало
OUT_LO_Shadow
Обнуляв OUT_H
E923 ldaa
E925 staa
E927 ldaa
E929 staa
TCR correction with
Cu wire (0.0043 1/K)
bbs.38hot.net


IC352
R301
BECKMAN
898-3-R47K
IC301
AD7533JN
8322
C306
OP97
F 102
G83736 B
IC602
TR503
D302
TR301
TP505
TP302
LK302
C302
R303
R309
74LS13
5A
bbs.38hot.net

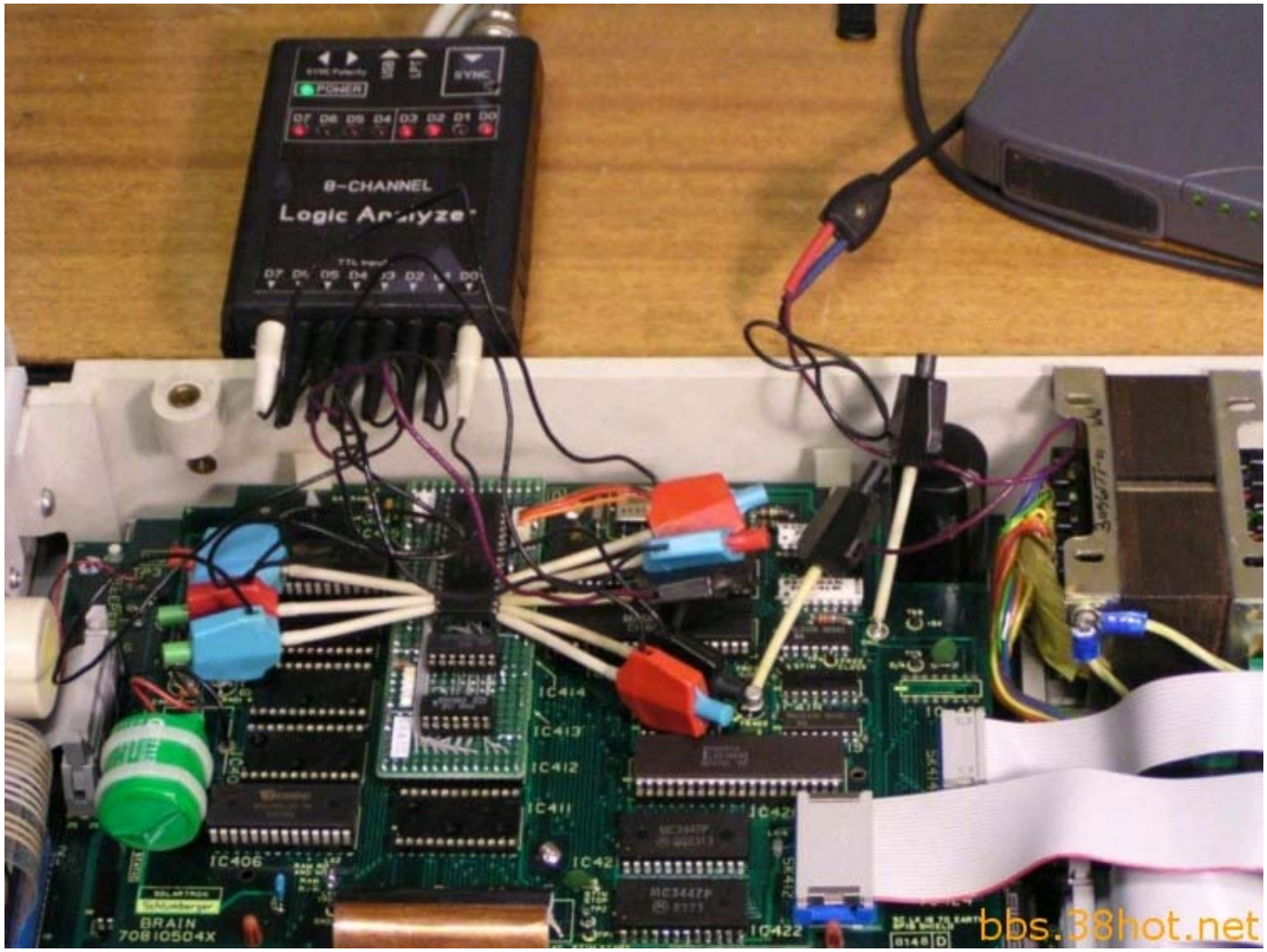


4) Finally, I'm found a serious lack of the Solartron 7081 design: improper function of the periodic drift correction (ADC Zero, AutoZero), that lead to large DC voltage measurement errors (discontinuities), up to 5-7 ppm at the all ranges. The source of this problem is very simple: PWM ADC full settling time is much more than specified 13 ms. But the problem solution is hidden in the Floating Logic processor's firmware (IC803 ROM). IC803 firmware contains all of the hardware-specific delays, registers look-uptables, two complicated finite-state machines, virtual software timers, software GLUGs integrator, inter-board messaging system interface, calibration NVRAM support e.t.c.


Solartron 7081 AutoZero bug
Normal measurement
Drift correction (ADC Zero) Cycle
Normal measurement
10 V
Measurement result
Settling
Error, up to 50-70 µV
6½
Wrong ADC Offset
7½
8½
True ADC Offset
Every ~ 15 min
6½
7½
8½
bbs.38hot.net



First of all I tried to build a Solartron 7081 processors IO/Memory maps and reconstruct inter-boards messaging system protocol. Then, within two weeks, I reversed the Floating Logic processor's firmware and drew one of the two Finite-State Machines. After that I wrote a patch code using the free areas at the end of the ROM space.


8-CHANNEL
POWER
SYNC
IC414
IC413
IC412
IC411
IC406
IC42
IC422
BRAIN
708105O4X
bbs.38hot.net

Earthy Logic I/O Map

Base address, hex	Devices
5C00	IC27 -> IC16 ?
5800	GPIB Address Switches
5400	PIA: Minate interface, NVClock, Beeper
5000	R/WQ, Floating UART
4C00	PIA: Keyboard, NVClock, Calibration key
4800	RS232
4400	GPIB I/O
4000	DMA Select

Floating Logic Memory Map

Address range, hex	Devices	
E000-FFFF	ROM	
C000-DFFF	Free space (no decoding)	
A000-A3FF, A400-A7FF	NVM pages	
8000-9FFF	Free space (no decoding)	
6000-7FFF	I/O space	
4000-5FFF	GLUG LO -	Read word at 3FFF-4000
2000-3FFF	GLUG HI - / Reset	
0000-1FFF	RAM, CPU internal registers and ports	

Floating Logic I/O Map

Port	6000h (OUT LO-)	6100h (OUT HI-)	6200h (OUT AC-)	6300 (OUT TC-)
bit 7	RATIO Control	RLD7 (protection)	AC	FRSS (6302h)
bit 6	I/P AMP Control	–	AC+DC	FAS (6304h)
bit 5	RATIO HI Control	RLD501 (TestK)	AC Filter	TC6
bit 4	Test0	RLD6 (in. Div100)	TestAC	TC5
bit 3	10 uA Control	RLD5 (in. InpAmp)	AC ?	TC4
bit 2	x100	RLD4 (Div100)	1	TC3

Earthy to Floating Processors messaging system

The basis of the Earthy and Floating Processors interface is a simple serial link and special messaging protocol. Serial link have a two selectable clocks: 76800 bauds for normal operation and 300 bauds for debug purposes.

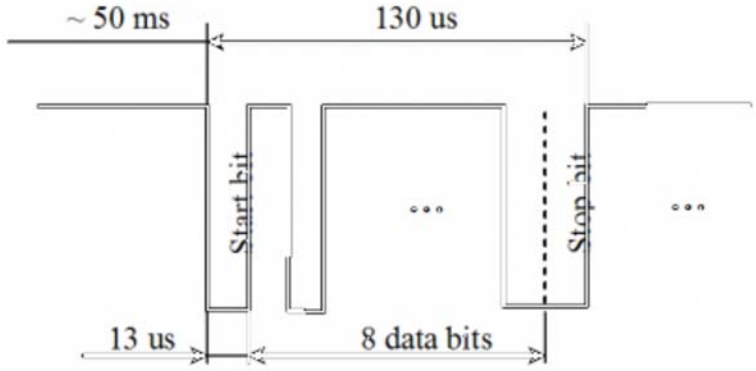
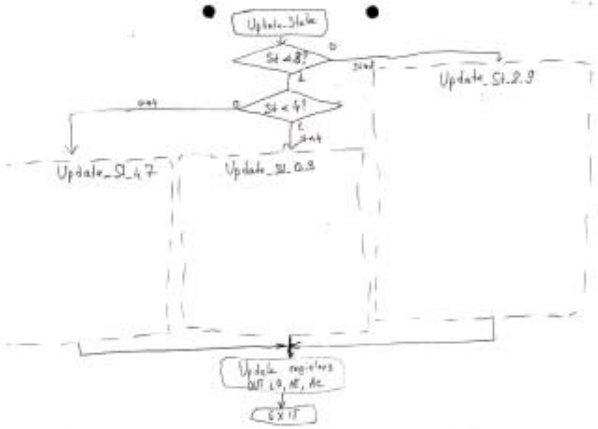


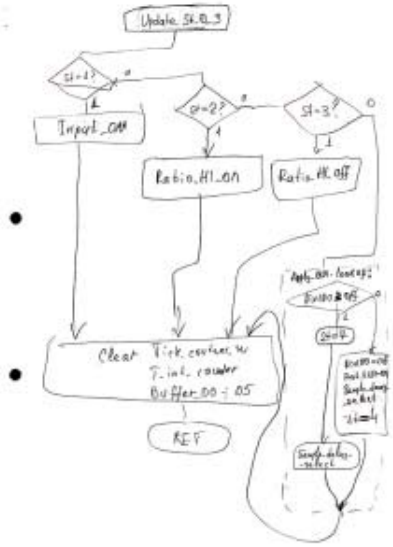
Table 1 – Single message structure

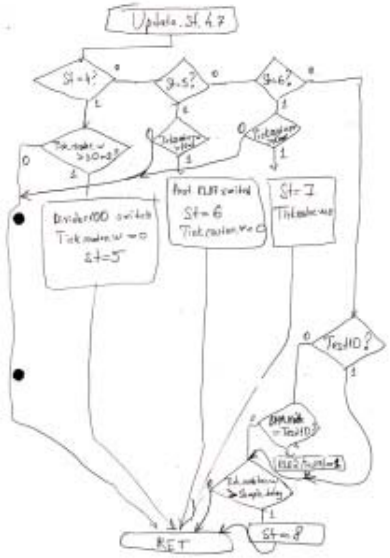
Byte #	1	2	3	4	5	6	7	8
Function	81h	CRC	Range	Mode	Nines	State	Cmd	8Dh

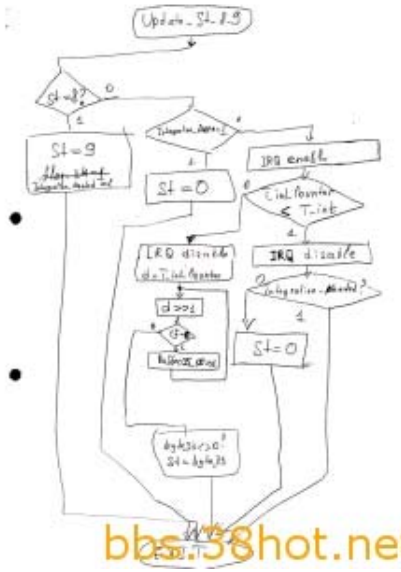
Byte #	Function	Description			
1	81h	Begin of the message flag / Message type			
2	CRC	Message checksum = 0FFh – sum(byte[3:8])			
3	Range	DMM Range selection. For DCV:			
		0 = Auto	1 = 0.1 V	2 = 1.0 V	3 = 10 V
		4 = 100 V	5 = 1000 V		
4	Mode	DMM Mode selection:			
		0 = VDC	1 = VAC	2 = Ohms	3 = VAC + VDC
		4 = Test0	5 = Test10	6 = TestK	7 = TestAC ?
		8 = Reference	9 = [1]+filt	0Ah = [3] + filt	0Bh = True Ohms
5	Nines	Integration time / Digits selection:			
		3 = 3x9	4 = 4x9	5 = 5x9	6 = 6x9

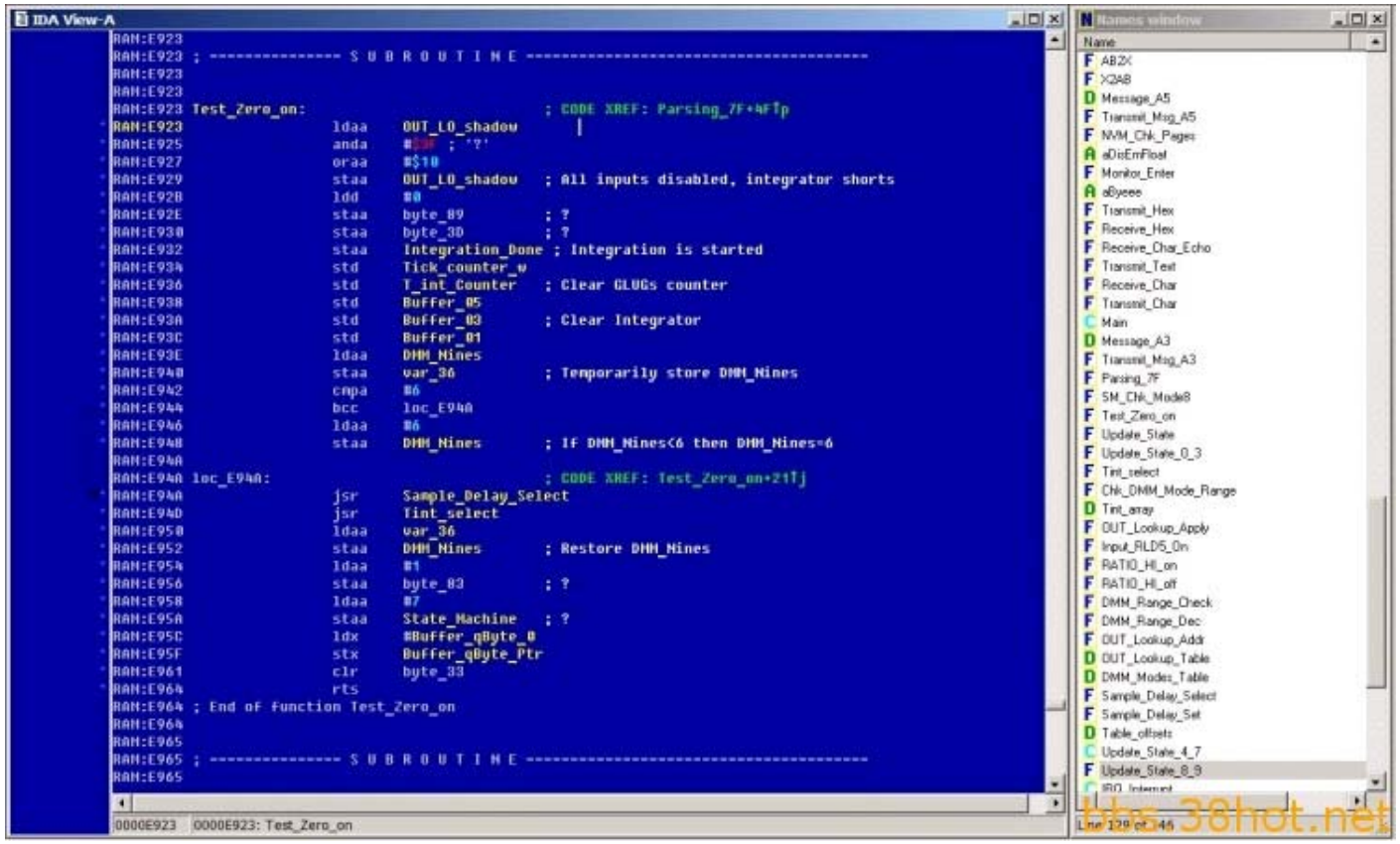
Solartron 7081
“Floating” Logic
Finite-state Machine №1










IDA View-A
RAM:E923
RAM:E923 ; ---------- S U B R O U T I N E ----------
RAM:E923 Test_Zero_on: ; CODE XREF: Parsing_7F+4F↑p
RAM:E923 ldaa OUT_LO_shadow
RAM:E925 anda #$DF ; 'ß'
RAM:E927 oraa #$10
RAM:E929 staa OUT_LO_shadow ; All inputs disabled, integrator shorts
RAM:E92B ldd #0
RAM:E92E staa byte_89 ; ?
RAM:E930 staa byte_3D ; ?
RAM:E932 staa Integration_Done ; Integration is started
RAM:E934 std Tick_counter_w
RAM:E936 std T_int_Counter ; Clear GLUGs counter
RAM:E938 std Buffer_05
RAM:E93A std Buffer_03 ; Clear Integrator
RAM:E93C std Buffer_01
RAM:E93E ldaa DMM_Nines
RAM:E940 staa var_36 ; Temporarily store DMM_Nines
RAM:E942 cmpa #6
RAM:E944 bcc loc_E94A
RAM:E946 ldaa #6
RAM:E948 staa DMM_Nines ; If DMM_Nines<6 then DMM_Nines=6
RAM:E94A
RAM:E94A loc_E94A: ; CODE XREF: Test_Zero_on+21↑j
RAM:E94A jsr Sample_Delay_Select
RAM:E94D jsr Tint_select
RAM:E950 ldaa var_36
RAM:E952 staa DMM_Nines ; Restore DMM_Nines
RAM:E954 ldaa #1
RAM:E956 staa byte_83 ; ?
RAM:E958 ldaa #7
RAM:E95A staa State_Machine ; ?
RAM:E95C ldx #Buffer_qByte_0
RAM:E95F stx Buffer_qByte_Ptr
RAM:E961 clr byte_33
RAM:E964 rts
RAM:E964 ; End of function Test_Zero_on
RAM:E965 ; ---------- S U B R O U T I N E ----------
0000E923 0000E923: Test_Zero_on
Names window
Name
ABZC
X2AB
Message_A5
Transmit_Msg_A5
NVM_Chk_Pages
aDisEmFloat
Monitor_Enter
aByeee
Transmit_Hex
Receive_Hex
Receive_Char_Echo
Transmit_Text
Receive_Char
Transmit_Char
Main
Message_A3
Transmit_Msg_A3
Parsing_7F
SM_Chk_Mode8
Test_Zero_on
Update_State
Update_State_0_3
Tint_select
Chk_DMM_Mode_Range
Tint_array
OUT_Lookup_Apply
Input_RLD5_On
RATIO_HI_on
RATIO_HI_off
DMM_Range_Check
DMM_Range_Dec
OUT_Lookup_Addr
OUT_Lookup_Table
DMM_Modes_Table
Sample_Delay_Select
Sample_Delay_Set
Table_offsets
Update_State_4_7
Update_State_8_9
bbs.38hot.net

Patch for Solartron 7081 Floating Processor ROM (VAF BSW 13 Fe 84)

Version 1.0b:

+ fixed AutoZero errata (wrong settling time)

Mickle T. aka iddqd2001 (Russia), 2011

Procedure Test_Zero_On (modified code)

ROM offset	*CPU offset*	*Opcodes*	*Mnemonics*
923	E923	86 00	ldaa 00h
925	E925	97 68	staa OUT_HI_Shadow
927	E927	BD F2 10	jsr Test_Zero_Patch
92A	E92A	01	nop
...	...	...	...
94A	E94A	BD F2 20	jsr Test_Zero_Patch2
...	...	...	...

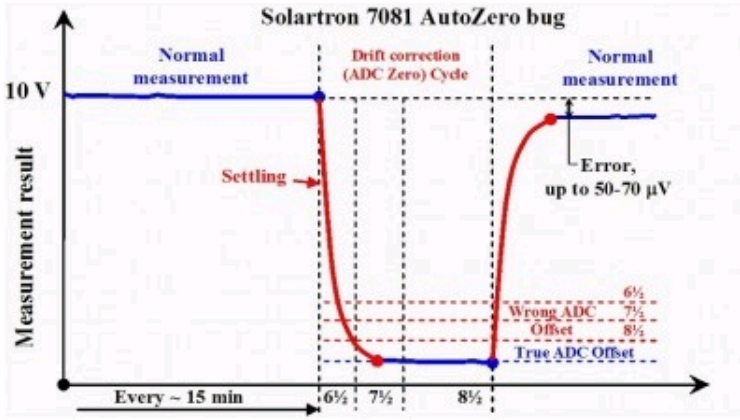
Procedure Test_Zero_Patch (new code)

ROM offset	*CPU offset*	*Opcodes*	*Mnemonics*
1210	F210	96 67	ldaa OUT_LO_Shadow
1212	F212	84 3F	anda 3Fh
1214	F214	8A 10	oraa 10h
1216	F216	97 67	staa OUT_LO_Shadow
1218	F218	39	rts

Procedure Test_Zero_Patch2 (new code)

ROM offset	*CPU offset*	*Opcodes*	*Mnemonics*
1220	F220	CC XX YY	ldd XXYY (Delay, ms) *
1223	F223	DD 3A	std Sample_Delay
1224	F224	39	rts

* For 3200 ms XX=0C, YY=80



OPTIONAL

Procedure Parsing_7F

ROM offset	*CPU offset*	*Opcodes*	
...	...	...	...
8AB	E8AB	C1 0D	Auto-Zero interval *
...	...	...	...

* Default 0Dh=15 min, 1=65.6 sec.

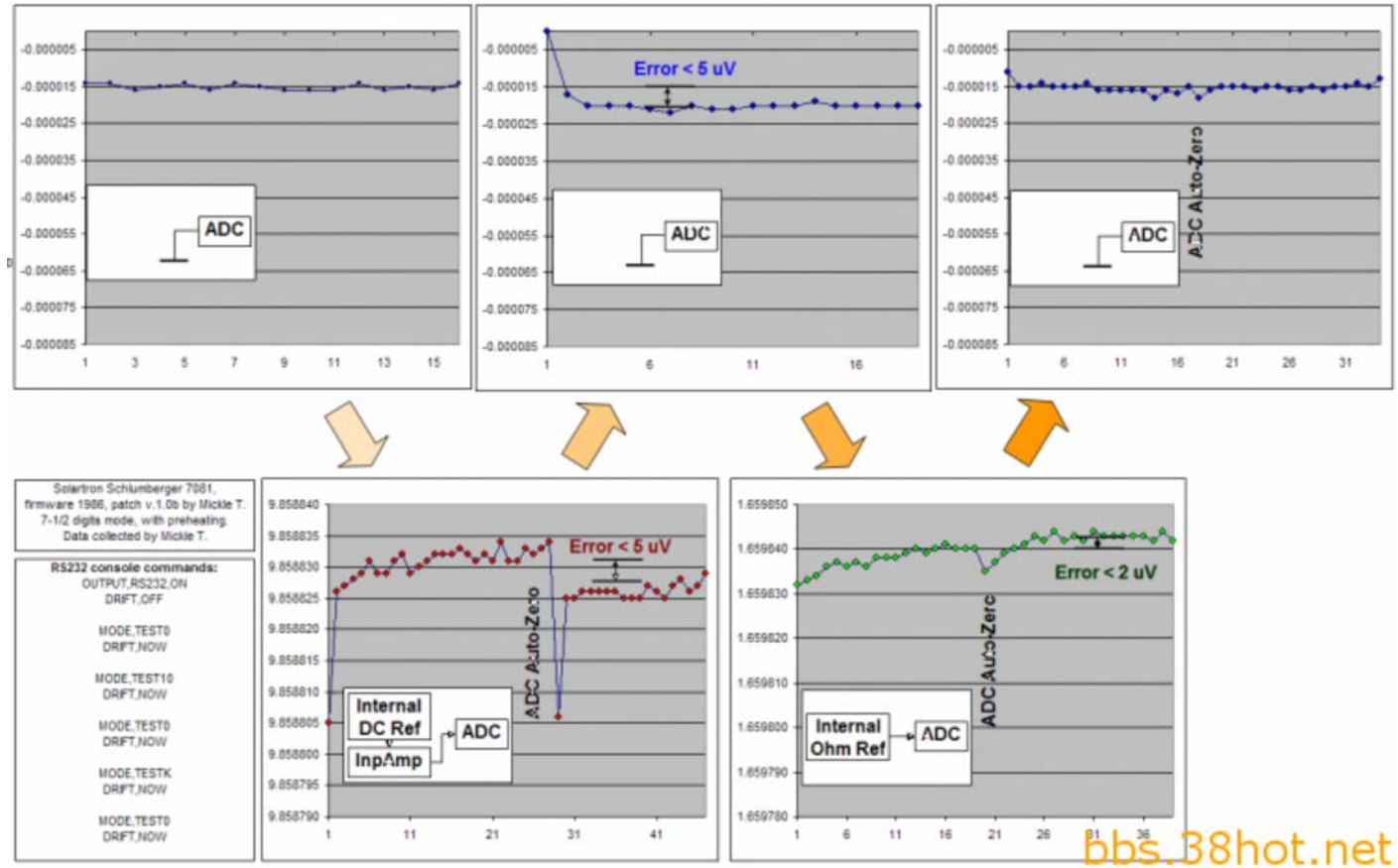
```
RAM:E893 Parsing_7F:                             ; CODE XREF: RAM:loc_E87BTP
RAM:E893                ldaa    byte_7F
RAM:E895                tst     byte_3E
RAM:E898                bne     loc_E8AF
RAM:E89A                cmpa    #3
RAM:E89C                beq     loc_E8BC         ; Jump if =3
RAM:E89E                ldab    DNM_Nines
RAM:E8A0                cmpb    #6
RAM:E8A2                bcs     loc_E8BC         ; Jump if DNM_Nines<6
RAM:E8A4                tst     TC_running_flag
RAM:E8A7                beq     loc_E8BC         ; Jump if Tick Counter stopped
RAM:E8A9                ldab    Tick_counter.hi_byte
RAM:E8AB                cmpb    #$D              ; ■■-Zero interval (15 min. default)
RAM:E8AD                bcs     loc_E8BC         ; Jump if less
RAM:E8AF
RAM:E8AF loc_E8AF:                               ; CODE XREF: Parsing_7F+5Tj
RAM:E8AF                clr     byte_3E
RAM:E8B2                cmpa    #4
RAM:E8B4                beq     loc_E8BC
RAM:E8B6                staa    byte_64
RAM:E8B8                ldaa    #4
RAM:E8BA                staa    byte_7F
```

ROM checksum!!!

ROM offset	*CPU offset*	*Opcodes*	
0000	E000	ZZ	Checksum additional constant: ZZ+sum(E000:FFFF)=0

http://www.fileserve.com/file/kctz34r/7081_Docs.rar
http://www.fileserve.com/file/G36ugDs/7081_IC803_patched.rar

Now, the problem is solved:



[iddqd2001 2012-01-08 18:12]

14 +42 +12

leobian	+3	n	2012-01-12
vr2whf	+1	Awesome! Learn a lots. Salute to you.	2012-01-12
default	+3	n	2012-01-10
gaobingic	+5	good job!I 'll study to repair a broken one!	2012-01-09
cuison	+5	very good! thank u share.	2012-01-09
csclz	+3	n	2012-01-08
	+3	n	2012-01-08
	+5		2012-01-08
lymex	+3	n	2012-01-08
lymex	+5	n	2012-01-08

1 2

New life of the Solartron 7081

hldiy

1 : 2012-01-08

1458
23034
134

http://shop62201038.taobao.com/

LM399AD588BQLTZ1000ltflu

iddqd2001

2 : 2012-01-08

Can't understand why appeared two last pictures in my post? Can't delete it 

100
334
38

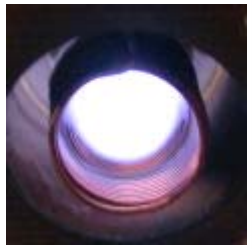
3 : 2012-01-08

1663
1823
5

4 : 2012-01-08

Move over the picture to be deleted, when the upper left corner box when prompted, choose the right [] either.

130 5885 1820 Q_Q 2 4 7 5 0 3 4
: ruching.wong@hotmail.com
[]



1062
1423
68

ruinedone

5 : 2012-01-08

google

Strongly recommend not using china phrase, which may blind google translate and then this our Russia friend.

254
363
1

iddqd2001

6 : 2012-01-08

, thank you! Extra pictures deleted!

No problem with Google Translate. With it I can understand more then 80% of posts.

100
334
38

7 : 2012-01-08

38

215
166
2

cdma

8 : 2012-01-08

Good good study day day up

587
22630
42

redtony

9 : 2012-01-08

!

:

2659
694
137

redtony

10 : 2012-01-08

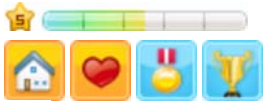
5

2659
694
137

xplore

11 : 2012-01-08

Great



824
869
46

mige062

12 : 2012-01-08

44
151
0

13 : 2012-01-08

Good article!

2323@163.com QQ:78520813

485
704
23

csclz

14 : 2012-01-08

n

888
11
35

38tt

15 : 2012-01-08

xplore

xplore:Great

(2012-01-08 20:00)

479
11442
0

7r093

16 : 2012-01-08

158
9089
4

iking921

17 : 2012-01-08

2590
1503238851
25

roller

18 : 2012-01-08

very interesting

but I wondered you have spent a lot time to repair this antique DMM is just for fun or it really can be used as an measuring instrument after repair?

I also like buy old instrument but i'd rather for keep them as antiques than use them as measuring instrument for their out of date hardware and software could not meet the requirement which an single chip would do

59
180
1

iking921

19 : 2012-01-08

xplore

xplore:Great

(2012-01-08 20:00)

2590
1503238851
25

1 2

Re:Solartron 7081 Repairing (continue)

100

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